DOCKET: FIS920000227US2 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR:	Divakaruni et al.	PRIOR EXAMINER:	Kin Chan Chen
SERIAL NO.:	Divisional Application of U.S. Serial No. 09/885,790	PRIOR ART UNIT:	1765
FILING DATE:		DATE:	November 25, 2003
FOR:	SELF-ALIGNED STI FOR NARROW TRENCHES		

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 CFR 1.56, 1.97 and 1.98, the following items are made of record to assist the Patent & Trademark Office in its examination of this application and is, in the opinion of the attorney designated below for applicant(s), information relevant to the closest prior art of which that person is aware:

PATENT NO.	***INVENTOR***	***ISSUE DATE***
5,895,253	Akram	04/20/1999
5,998,251	Wu et al.	12/07/1999
6,030,867	Chien et al.	02/29/2000
6,265,302	Lim et al.	07/24/2001
6,344,383	Berry et al.	02/05/2002

PUBLICATIONS

"A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb", U. Gruening et al., IEDM 99-25, 1999.

"Extending Trench DRAM Technology to 0.15μm Groundrule and Beyond", T. Rupp et al., IEDM 99-33, 1999.

"A 0.135 μm^2 $6F^2$ Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", C. J. Radens et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 80-81, IEEE, 2000.

Each of the foregoing items has either been disclosed or cited in the parent application Serial No. 09/885,790 filed on June 20, 2001. The instant application relies on U. S. Serial No. 09/885,790 for an earlier filing date under 35 USC § 120. Therefore, pursuant to 37 CFR § 1.98 (d), applicants are not submitting copies of the aforementioned items. A form 1449 is enclosed herewith.

Respectfully submitted,

Kelly M. Reynolds
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CERTIFICATION OF MAILING UNDER 37 CFR 1.10

"Express Mail" mailing label number EV332850982US Date of Deposit: November 25, 2003 I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner for Patents and Trademarks, Washington, D.C. 20231

Name: Carol M. Thomas Date: November 25, 2003 Signature:

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.: FIS920000227US2	Divisional Application of U.S. Serial No.: 09/885,790
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT: Divakaruni et al.	
(Use several sheets if necessary) (37 CFR 1.98(b))	FILING DATE:	PRIOR ART GROUP: 1765

REFERENCE DESIGNATION — U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	AA	5,895,253	04/20/1999	Akram			
	AB	5,998,251	12/07/1999	Wu et al.			
	AC	6,030,867	02/29/2000	Chien et al.			
	AD	6,265,302	07/24/2001	Lim et al.			
	AE	6,344,383	02/05/2002	Berry et al.			
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

			PUBLICATION	COUNTRY OR		SUB-	TRANSLATION	
		DOCUMENT NUMBER	DATE	PATENT OFFICE	CLASS	CLASS	YES	NO
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	"A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb", U. Gruening et al., IEDM 99-25, 1999.
	AR	"Extending Trench DRAM Technology to 0.15μm Groundrule and Beyond", T. Rupp et al., IEDM 99-33, 1999.
	AS	"A 0.135 μm^2 $6F^2$ Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", C. J. Radens et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 80-81, IEEE, 2000.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.